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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,732	07/30/2004	Ko-Hsing Chang	13041-US-PA	4731

31561 7590 10/08/2008

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
HARRISON, MONICA D	
ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
10/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW
Belinda@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/710,732	CHANG ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-20* is/are allowed.

6)☒ Claim(s) *1-12, 14, 15* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's request for continued examination filed 5/9/08 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes (6,611,037 B1) in view of Shibib (6,228,750 B1).

2. Regarding claim 1, Rhodes discloses a method o£ fabricating a photodiode, comprising the steps of: providing a substrate (Figure 6, reference 316); forming a well region of a first conductive type in the substrate (Figure 6, reference 311); forming an isolation structure in the substrate to define a photosensitive area on the substrate (Figure 6, reference 350), and forming a plurality of trenches in the well region of the substrate within the photosensitive area (Figure 6, reference 324). However, Rhodes does not disclose depositing a doped layer of a. second conductive type over of the first conductive type in the substrate, wherein the doped layer covers the interior wails of the trenches and the surface of the well region of the first conductive type in the substrate within the photosensitive area.

Shibib discloses depositing a doped layer of a. second conductive type over of the first conductive type in the substrate, wherein the doped layer covers the interior wails of the trenches and the surface of the well region of the first conductive type in the substrate within the

photosensitive area, and the doped layer and the well region thereunder together form the photodiode (Figure 1C, reference 107; column 3, line 26).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Rhodes with the teachings of Shibib for the purpose of doping a semiconductor surface to form a photodiode.

3. Regarding claims 2 and 12, Shibib discloses wherein after the step of forming the doped layer over the substrate, further comprises performing an annealing operation (Figure 1D, column 3, line 43).

4. Regarding claim 3, Shibib discloses wherein the annealing operation drives the dopants within the doped layer of the second conductive type into the substrate and make junction of the first conductive type and the second conductive type shift into the substrate (Figure 1D, column 3, line 43).

5. Regarding claim 4, Shibib discloses wherein the first conductive type is P-type and the second conductive type is N- type (Figure 1E).

6. Regarding claim 5, Rhodes discloses wherein the first conductive type is N-type and the second conductive type is P-type (Figure 14, references 315 and 340).

7. Regarding claim 6, Rhodes discloses wherein the step of forming the doped layer comprises performing a chemical vapor deposition process (column 12, lines 65-67 thru column 13, lines 1-9).

8. Regarding claim 7, Rhodes discloses wherein a material constituting the doped layer is selected from the group consisting of doped polysilicon and doped epitaxial silicon (Figure 14, reference 340; *doped polysilicon*).

9. Regarding claims 8 and 15, Rhodes discloses wherein the doped layer completely fills the trenches (Figure 14, reference 340).

10. Regarding claim 9, Rhodes discloses forming a buffer layer over the substrate covering the interior walls of the trenches as well as the surface of the substrate within the photosensitive area after forming the trenches in the substrate within the photosensitive area (Figure 11, reference 328).

11. Regarding claim 10, Rhodes discloses wherein the step of forming the buffer layer comprises performing a chemical vapor deposition process (column 10, lines 49-65).

12. Regarding claim 11, Rhodes discloses wherein a material constituting the buffer layer is selected from the group consisting of polysilicon and epitaxial silicon (column 10, lines 48-65).

13. Regarding claim 14, Shibib discloses wherein the annealing operation drives the dopants within the doped layer into the well region of the substrate so that a junction of the second conductive type and the first conductive type is formed within the well region of the substrate (Figure 1D, column 3, line 43).

Allowable Subject Matter

14. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. Claims 16-20 are allowed over the prior art of record.

Reasons for Allowance

16. The following is an examiner's statement of reasons for allowance: The prior art does not disclose nor fairly suggest a method for fabricating a photodiode as described in claim 13 wherein after forming the doped laver over the substrate, an annealing operation is performed to drive the dopants within the doped layer into the buffer layer so that a junction of the second conductive type and the first conductive type is formed within the buffer layer an in the context of its related claims nor a method of fabricating a photodiode as described in independent claim 16, including forming a buffer layer of a semiconductor material over the well region, forming a doped layer of a second conductive type directly over the buffer layer, and performing an annealing operation.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

17. Applicant's arguments filed 5/9/08 have been fully considered but they are not persuasive. Rhodes along with Shibib still read on applicant's instant application in its entirety. Applicant's amendment to claim 1 does not overcome the previous rejection. Shibib discloses depositing a doped layer of a second conductive type over of the first conductive type in the substrate, wherein the doped layer covers the interior wails of the trenches and the surface of the well region of the first conductive type in the substrate within the photosensitive area, and the

doped layer and the well region thereunder together form the photodiode (Figure 1C, reference 107; column 3, line 26).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica D. Harrison/
Examiner, Art Unit 2893

mdh
September 29, 2008

/Davienne Monbleau/
Supervisory Patent Examiner, Art Unit 2893